C. REMARKS

Status of the Claims

Claims 1, 3-8, 11, 13, 15-18, 20, and 22-30 are currently present in the Application, and claims 1, 11, 18, and 25 are independent claims. Claim 18 has been amended, no claims have been canceled, and no claims have been added in this response.

Examiner Interview

Applicants note with appreciation the telephonic interview conducted between Applicants' representative and the Examiner on February 7, 2007. During the telephonic interview, the Examiner and Applicants' representative discussed the 102 reference (Auslander et al., Patent No. 6,601,146). In particular, Applicants' representative discussed that Applicants' invention shares a common memory map between two different **processors** to access a common memory, whereas Auslander discloses a method for sharing a common memory map between two different **processes** that reside on a single processor to access a common memory. Applicants' representative discussed that when Auslander's processes reside on different processors, Auslander uses **different** memory maps for each of the different processors to access the shared memory. No agreement was reached regarding the claims.

Claim Rejections

Claims 1, 3-8, 11, 13, 15-18, 20, and 22-30 stand rejected under 35 U.S.C. § 102 as being anticipated by Auslander et al. (U.S. Patent No. 6,601,146, hereinafter "Auslander"). Applicants respectfully traverse these rejections.

Applicants' claim 1 is directed towards a memory shared by a plurality of heterogeneous processors with limitations comprising:

- the shared memory;
- wherein the shared memory is accessible by one or more first processors that are adapted to process a first instruction set;
- wherein the shared memory is accessible by one or more second processors that are adapted to process a second instruction set; and
- a memory map corresponding to the shared memory, wherein the memory map includes cross-references between virtual addresses and real addresses and is **shared between the first processors and the second processors.**

Claim 1 includes a limitation of a memory map that is "*shared between the first processors and the second processors.*" Applicants' first and second processors use the same architectural address translation mechanism, and thus use the same cross-references between virtual addresses and real addresses, to access a common memory. Applicants' Figure 44A shows that processing unit 4430 and synergistic processing unit 4405 share the same system memory map 4420.

Auslander discloses a method for **processes** to share a common memory map when they reside on a single processor, but never teaches or suggests these processes sharing the same memory map when they reside on different **processors** as claimed by Applicants. Auslander states:

> "This invention provides for an inter-process communication transfer region having a unique physical address, where the region is shared among all processes on **a given processor** of a computer system. This unique physical address is then mapped into a virtual address in the address space of each of the processes. When a first of the processes needs to transfer data to a second of the process, the first

> process stores arguments describing the data in the region. When a second of the processes needs to receive the data, the second process reads the data from the region by **using a second virtual address in its address space** which maps into the unique physical address." (col. 2, line 58 through col. 3, line 2, emphasis added)

Auslander's Figure 2 shows a virtual address space of a client (19a), a virtual address space of a server (19b), and the shared memory (20). Figure 2 shows that the client and the server use different memory maps to access the shared memory, which are mapping 15a (client memory map) and mapping 15b (server memory map). As can be seen, these two memory maps are quite different. First, the virtual address space of mapping 15a (client) locates "Region 1" between "Region 0" and "Region N," whereas the virtual address space of mapping 15b (server) locates "Region 1" between "IPC Region" and "Region' N." Second, mapping 15a's "Region 1" is mapped to a different physical location on shared memory 20 than mapping 15b's "Region' 1." If Auslander did teach that the client and server share the same memory map, mapping 15a and mapping 15b would be identical, which they are not.

During the Examiner interview, the Examiner pointed to an excerpt from Auslander that states:

> "When process A (a client) wishes to communicate with process B (a server), process A makes a (cross address space) procedure call to process B. The data that is communicated is stored as arguments of the function call…" (col. 5, lines 24-26)

Although the excerpt discusses transferring data from a client to a server, the excerpt never teaches or suggests the client and the server sharing the same memory map. As discussed above and shown in Auslander's Figure 2, the client's memory map and the server's memory map are, in fact, different. As such,

Auslander never teaches or suggests "*a memory map corresponding to the shared memory, wherein the memory map includes cross-references between virtual addresses and real addresses and is* ***shared between the first processors and the second processors***" as claimed by Applicants.

Therefore, since Auslander does not teach all of the limitations included in Applicants' claim 1, claim 1 is allowable over Auslander. Independent claim 11 is a method claim including similar limitations of claim 1 and, therefore, is allowable for at least the same reasons as claim 1 is allowable.

Applicants have amended the preamble of independent claim 18 in order to avoid receiving a 101 rejection in subsequent Office communications. Independent claim 18 is a computer program product claim including similar limitations of claim 1 and, therefore, is allowable for at least the same reasons as claim 1 is allowable. Independent claim 25 is a system claim including similar limitations of claim 1 and, therefore, is allowable for at least the same reasons as claim 1 is allowable.

Notwithstanding the fact that claim 30 depends upon claim 1 and, therefore, is allowable for at least the same reasons as claim 1 is allowable, claim 30 adds limitations to claim 1 of:

- wherein the shared memory, the first processors, and the second processors are included on **one silicon substrate** and are connected using an **on chip coherent multi-processor bus.**

Applicants' invention resides on one silicon substrate, and an on chip coherent multi-processor bus connects the first processor, the second processor, and the shared memory. In contrast, Auslander never teaches or suggests such limitation in any part of Auslander. Auslander's Figure 4 shows a single processor 44, but never discloses that two heterogenous

processors, a common memory, and an on chip coherent multi-processor bus reside on one silicon substrate as claimed by Applicants.

Therefore, since Auslander never teaches or suggests all the limitations included in Applicants' claim 30, claim 30 is allowable over Auslander.

Each of the remaining claims 3-8, 13, 15-17, 20, 22-24, and 26-29 depends, either directly or indirectly, upon one of the allowable independent claims 1, 11, 18, or 25. Therefore, claims 3-8, 13, 15-17, 20, 22-24, and 26-29 are allowable for at least the same reasons that their respective independent claims are allowable.

Conclusion

As a result of the foregoing, it is asserted by Applicants that the remaining claims in the Application are in condition for allowance, and Applicants respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner contact the Applicants' attorney listed below if the Examiner believes that such a discussion would be helpful in resolving any remaining questions or issues related to this Application.

Respectfully submitted,

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